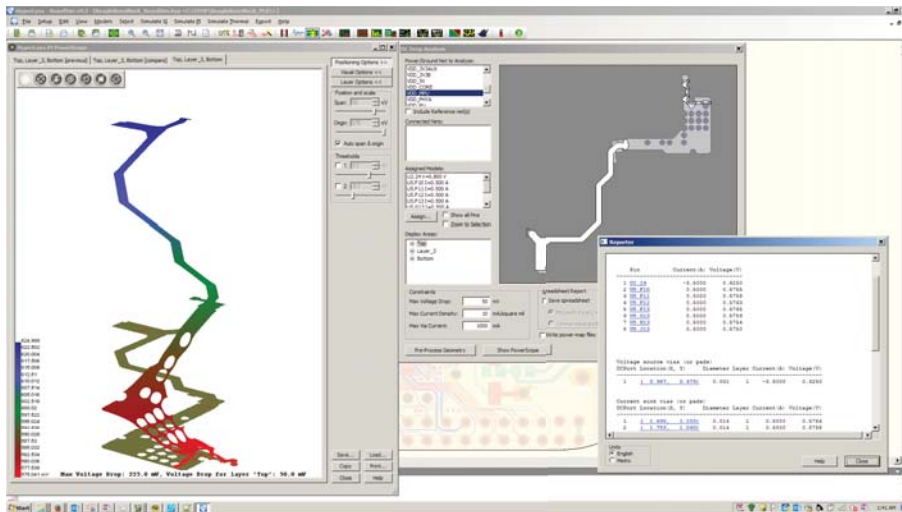




Advanced Analysis Option For PADS Professional



Use DC Drop analysis to prevent IC malfunction by identifying potential DC power-delivery issues such as excessive voltage drop.

OVERVIEW

PADS® Professional offers an Advanced Analysis option for PCB designers, engineers, and simulation specialists who need broad simulation capabilities. Advanced Analysis includes Power Integrity (PI) simulation and extended Signal Integrity (SI) planning and verification capabilities, including DDRx, powered by HyperLynx®.

Power integrity analysis is an essential part of modern electronic design. The number of voltages being used by ICs, plus increased current consumption, makes power delivery a difficult task. Compounding these issues are reduced layer counts, smaller noise margins, and increasing operating frequencies. With inadequate power delivery, designs exhibit signal integrity errors which can cause the logic on the board to fail.

Signal integrity and timing verification for DDR interfaces is critical. Most engineers do some DDR design and thus have a need to validate electrical performance. PADS provides a complete, integrated solution for DDR, DDR2, DDR3, and DDR4 verification as well as the low power counterparts, making it easy to run full batch analyses of DDRx designs.

The advanced analysis option for PADS Professional will help you design better-quality products and reduce product failures, quickly and efficiently.

MAJOR BENEFITS:

- Intuitive and easy to use for occasional and expert users
- Accurate modeling of signal interconnects and power delivery system
- Industry's fastest voltage drop and current density analysis of power supply rails
- Allows detailed 'what-if' exploration for constraint generation and post route signoff analysis
- Verifies DDRx interfaces including comprehensive signal quality and timing analysis
- Generates comprehensive reports
- Advanced crosstalk simulation to validate signal quality

POWER INTEGRITY ANALYSIS

Anyone can use HyperLynx PI, without weeks of software training. Advanced Analysis can identify power distribution problems early in the design, even prior to layout.

You can also identify design problems that would be difficult to identify in the lab and investigate solutions in an easy-to-use “what-if” environment. Once the layout is complete, validate the results to ensure that appropriate guidelines were followed. This reduces prototype spins and gets higher quality to market faster.

Analyze Voltage Drop

Prevent IC problems caused by DC power-delivery issues such as excessive voltage drop. Prevent damage by identifying high current density areas. All simulation results can be viewed in graphical and report format, making problems quick and easy to identify.

SIGNAL INTEGRITY FOR DDRx DESIGN

The Advanced Analysis option for PADS Professional provides powerful analysis of DDR-based designs to greatly reduce design and debug cycles. By accounting

for board-level effects such as inter-symbol interference (ISI) and crosstalk you can characterize signal-quality parameters such as setup and hold times, over/undershoot, monotonicity, etc. to validate against JEDEC standards or custom requirements. Advanced Analysis greatly reduces the setup time required to start your simulation, without sacrificing the detailed analysis required to make decisions about your design.

DDRx Design Creation

PADS Professional lets you create and validate designs incorporating high-speed parallel DDRx channel standards, the most common architecture for memory in the electronics industry.

DDRx in PADS supports all popular DDRx design standards from LPDDR-based designs found in mobile devices (including LPDDR4) to DDR4 SDRAMs found in high-end servers. You can perform pre-layout analysis to determine the best topology, or perform post-layout analysis to validate a single or multi-board system. PADS lets you easily import data from major CAD board layout sources, including Allegro®, making your work easy and efficient.

The screenshot displays the PADS Professional software interface. On the left, the 'Set Additional Simulation Options' dialog box is open, showing various simulation parameters such as 'Select IC model corners', 'Maximum run-time per net', and 'AC threshold selection'. The main window shows a 'Data Read Worstcases' report with the following table:

#	Signal	Accessed DRAM	Status	Setup Margin [ps]	Hold Margin [ps]
1	DDR_D0	U12 E3	Pass	132.5	75.8
2	DDR_D1	U12 F7	Pass	119.2	80.5
3	DDR_D10	U12 C6	Pass	151.1	19.3
4	DDR_D11	U12 C2	Pass	177.9	21.4
5	DDR_D12	U12 A7	Pass	173.8	22.2
6	DDR_D13	U12 A2	Pass	168.5	32.0

The interface also shows a waveform plot and a circuit board layout view.

Advanced analysis in PADS includes a complete, integrated solution that allows verification of DDRx memory systems, making it easy to run full batch analyses for timing and SI.

DDRx Analysis and Simulation

The validation of a DDRx bus involves the analysis of several timing and voltage measurements. Manual analysis of an entire DDR bus is impractical and can require more time than is typically available. The DDRx Wizard solves a major challenge in validating these design by automating the analysis of the vast number of parallel lines for nuanced signal integrity requirements.

With PADS you can automatically incorporate JEDEC requirements for validation, including waveform-shape dependent derating. PADS lets you customize validation

parameters, often needed at controllers, and conduct sweeps to run several “what-if” scenarios. DDRx in PADS also includes read and write leveling/calibration capabilities of the controller and non-ideal power source effects with IBIS 5.0 compatible models.

Advanced analysis in PADS further enhances your SI abilities by adding capabilities for loss modeling, advanced via modeling, eye diagrams, and multi-board analysis, giving you everything needed to get your products to market quickly, with higher quality and fewer design errors.

For the latest product information, call us or visit: www.pads.com

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