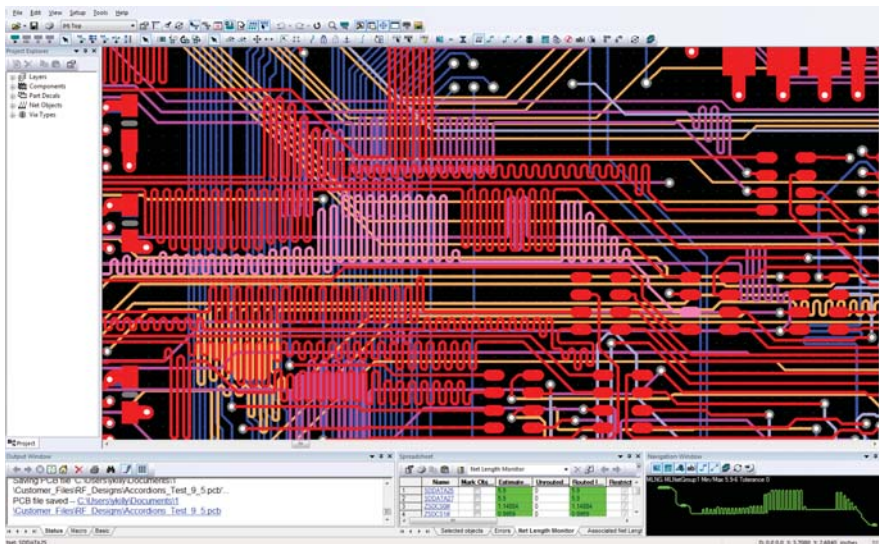




PADS Standard Plus Advanced PCB Option



The Advanced PCB Option for PADS Standard Plus automatically adds accordion patterns for nets with length constraints.

FEATURES AND BENEFITS:

- Saves time by automatically routing high-speed constrained nets.
- Ensures 100% testability for all nets on your board.
- Easily designs and places bare-die components on chip-on-board and multi-chip modules, ball grid arrays, and chip-scale packages.

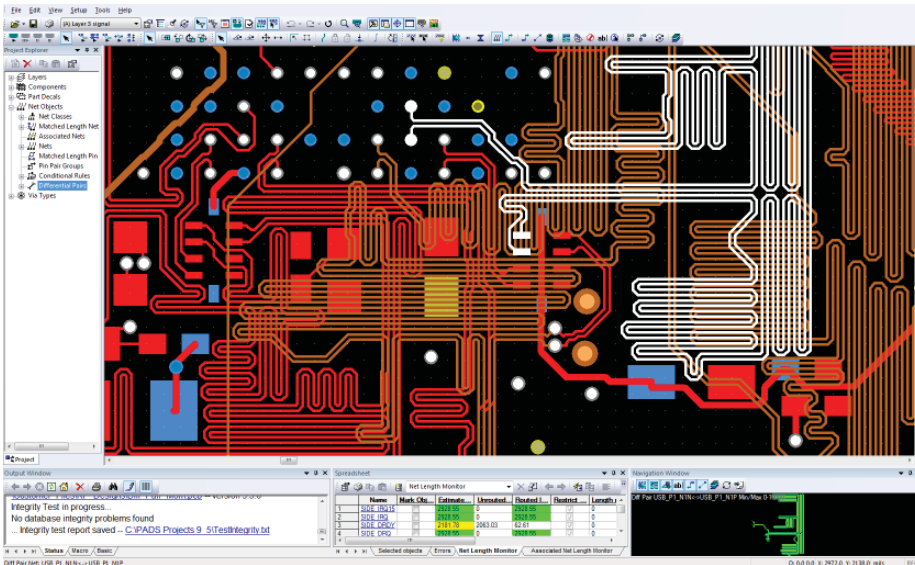
OVERVIEW

Extend your design capabilities with the Advanced PCB Option, available only with PADS® Standard Plus. The option includes best-in-class high-speed routing, time-saving DFT audit, and an advanced packaging toolkit for designing with bare-die components. Together, these capabilities will help you get your design done faster and more accurately, while reducing design and manufacturing costs.

High-Speed Routing

The Advanced PCB Option adds automatic high-speed routing to PADS Standard Plus. With it, you can autoroute length-constrained nets such as max/min and matched-length nets anywhere in the rules hierarchy. For example, you can assign net rules at the net or class level, and assign pin-pair rules at the group and pin-pair level. Matched-length rules can be set at the net, class, group, or pin-pair level.

You'll also be able to route with diagonal (135°) trace corners to eliminate undesirable impedance changes caused by sharp (90°) corners and help ensure the correct routing of length-constrained nets.



Automatically maintain differential pair rules including gap and length constraints.

Differential pairs are critical to high-speed design, allowing you to control signal skew, timing windows, and susceptibility to interference. The Advanced PCB Option maximizes these noise-canceling effects automatically and keeps the differential pair signals together for as much of the routing path as possible. Class-to-class clearances are followed according to the differential-pair settings you made in layout. You can even assign different design rules for differential pair gap and width according to layer.

Design for Test

The Advanced PCB Option's Design for Test (DFT) capabilities ensure the manufacturability of your design before you release it to fabrication.

To ensure testability, designs are audited through a series of analysis and verification checks performed on testpoints that have been added automatically or manually during the design phase. Testpoint definitions and parameters can be exported later and used in in-circuit test equipment. Any testability rule violation concealed in your design will be located, identified, and fixed in a matter of minutes.

PADS helps ensure the integrity of your designs by supporting testpoint insertion and locking. This helps

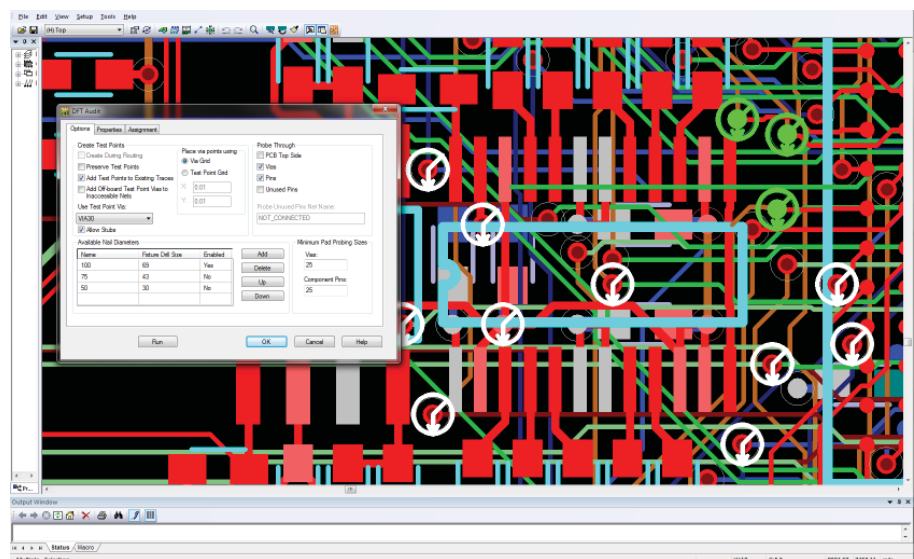
preserve test fixtures by maintaining previous testpoint locations and associated probe sizes throughout the lifecycle of the design. Graphical indicators make it easy to identify testpoint locations visually.

With control over testpoint rules, you can mirror the rules used in Automated Test Engineering (ATE), such as probe-to-probe, probe-to-component, probe-to-trace, probe-to-pad and probe-to-board clearances.

A simple user interface lets you simulate a multi-pass environment by defining different probe types to be included or excluded.

With the Advanced PCB Option, you can audit a "window area" or the entire PCB. DFT will recognize complex testpoint-keepout areas, and you can simulate the exact requirements ATE engineers use prior to committing a design to fabrication. You can also generate a comprehensive testpoint-coverage report for design review at any time.

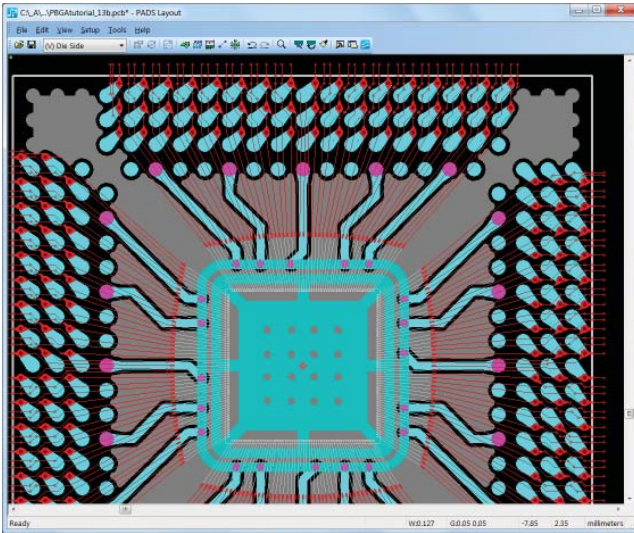
PADS manufacturing prep leverages the knowledge base existing in the ATE environment to perform DFT audits directly on your PCBs based on user-, product-, or corporate-defined test strategies.



DFT audit reduces costly design iterations and ensures the testability of your designs before fabrication.

Designing with Bare Die

Significantly reduce package design time and improve your PCB design quality with PADS advanced packaging tools, included in the Advanced PCB Option. Easily design and place bare-die components on chip-on-board (COB) and multi-chip modules (MCM), ball grid arrays (BGAs), and chip-scale packages (CSPs). Wizards allow you to automate key aspects of the package design process, including die capture, rules-based wire bond design, and flip-chip definition to improve the quality of your final design.



With the PADS Advanced PCB Option, you can reduce design time when designing with bare-die components.

Die Wizard

Use the PADS die wizard to quickly capture bare-die information, either through text or GDSII files or parametrically, using dialog boxes. Advanced filtering and preview capabilities help extract die-specific data easily. All chip-bond pad information will be read by the die wizard, including pad number, location, function, and pad shape and size.

The wizard's construction templates allow you to add missing data or to override imported data, such as die size or pad shape. Dynamic preview capabilities provide immediate graphical feedback during construction.

Die Flag Wizard

The die flag wizard automatically creates die flags, rings, and their associated solder mask openings, simplifying design creation. Immediate graphical feedback is provided as parameters are entered and modified.

PADS reduces design time by specifying the overall die-flag size relative to the selected die. Choose from predefined outer shapes, specify net association, and define the number of spokes and orientation. You can also specify paddle coverage, separate control rings, and define spoke width during parametric construction.

Wire Bond Wizard

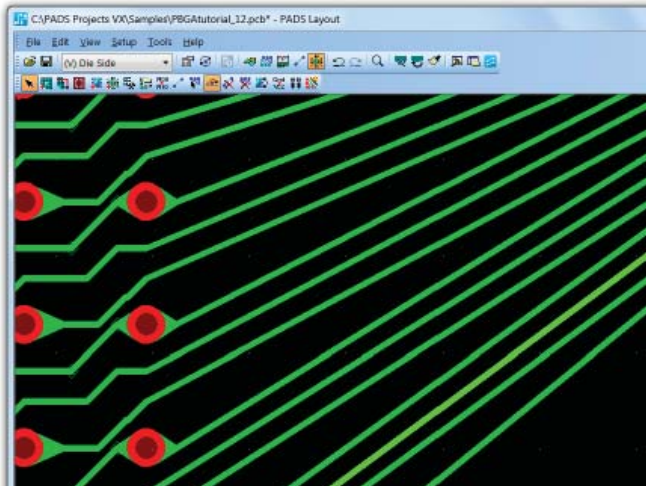
Also included in the Advanced PCB Option is a wire bond wizard which defines rules-driven automatic wire-bond fanout for easy evaluation of routability and substrate bond pad placement trade-offs. Parameters and constraints are presented in logical groups for simplified setup and iterative exploration. If insufficient area precludes the wizard from placing the bond pads according to the constraints, substrate bond pads will be placed and all violations reported. This makes it easy to experiment with alternative strategies while visualizing the results.

The Advanced PCB Option supports multi-row bond fanouts with unlimited wire-bond guides. All ring definitions and parameters can be saved for reuse in other designs to minimize setup time.

Route Wizard

An easy-to-use route wizard combines any-angle routing with pattern recognition to automatically route single-die advanced packages. By optimizing connections based on the configurations of the grid-array fanout and plating tail, the route wizard eliminates manual routing between a die and the package pins. Reduce design time with automatic routing of die quadrants and sides, to make package design with multiple dies easy.

The wizard automatically synthesizes connections between a bare die and a specific package layout, enabling collaboration between the packaging engineer, the IC engineer, and the board designer.



Interactive route editing supports any-angle routing to substrate pads, with or without a netlist.

The route wizard also quickly determines package feasibility based on the die and a set of technology rules. Once established, automatic routing completes and optimizes the design for manufacturing, eliminating time spent in planning and manually routing.

Report Generation

The Advanced PCB Option also enables PADS to automatically generate table-formatted documentation necessary for manufacturing and test.

Summary

Add the PADS Advanced PCB Option to your seat of PADS Standard Plus to dramatically decrease time-to-volume production, reduce costs, and improve product quality. With this option you can:

- Save time by automatically routing high-speed constrained nets.
- Ensure 100% testability for all nets on your board.
- Easily design and place bare-die components on chip-on-board and multi-chip modules, ball grid arrays, and chip-scale packages.

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