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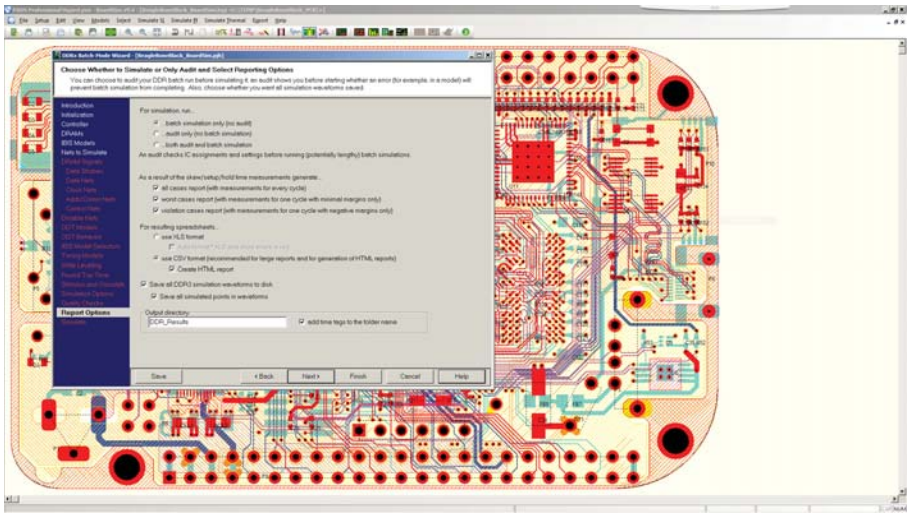
PADS HyperLynx DDR Option

For PADS Standard and PADS Standard Plus



The simple wizard-based interface makes it easy to set up DDR1/2/3 simulations.

MAJOR BENEFITS:

- Wizard-based interface helps analyze DDR1, DDR2, and DDR3 designs, including low-power variants
- Simulate with any number of DRAM devices, from single-memory to multiple-memory modules/slots
- Characterize Signal Integrity (SI) and system-level timing with setup/hold and derating calculations per JEDEC or custom standards
- Includes an HTML-based report with details of timing and SI results
- Allows an offline interactive view of simulation data

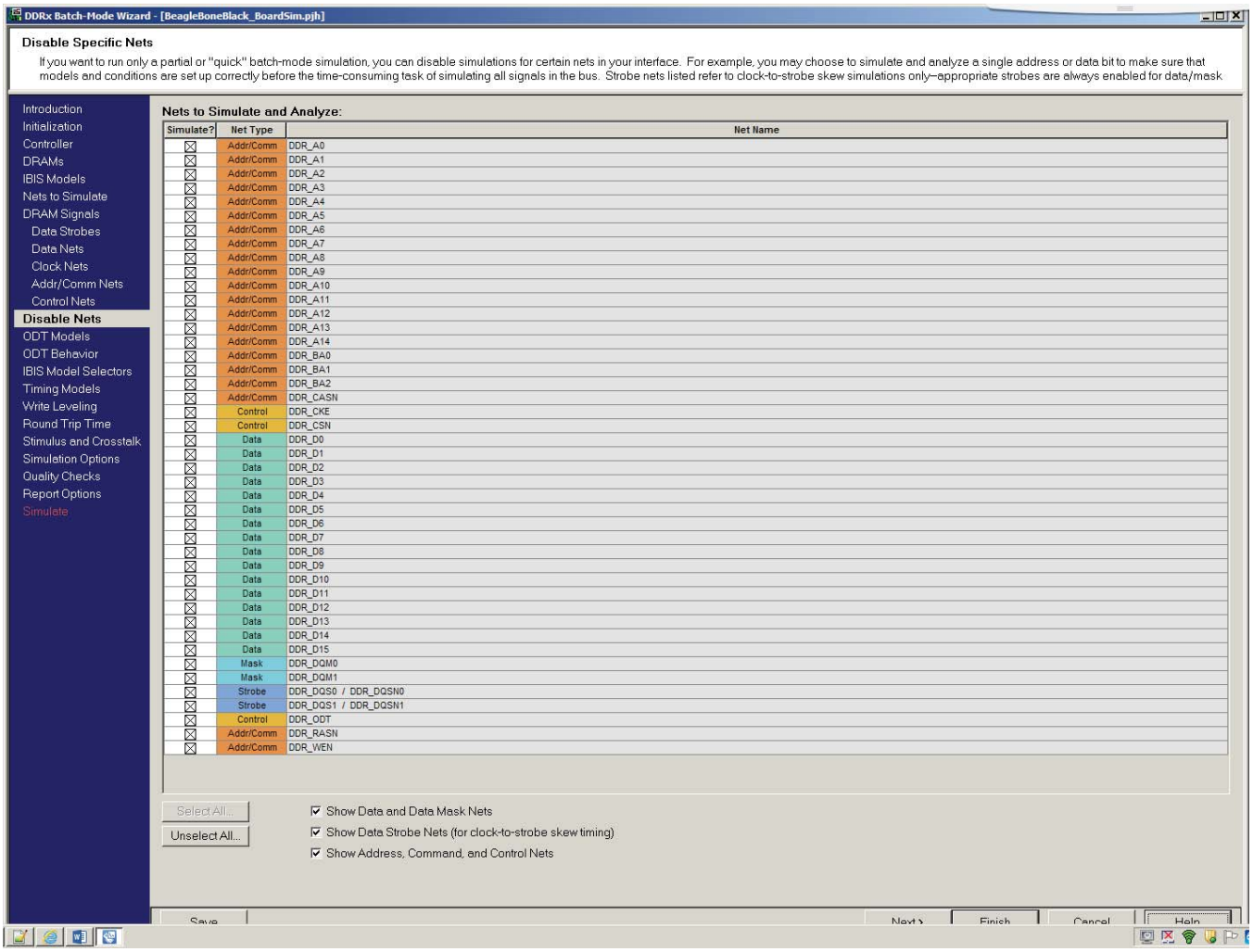
OVERVIEW

The PADS HyperLynx DDR option provides powerful analysis for PCBs with DDR memory, greatly reducing validation and debug cycles. Easily report setup/hold times, overshoot/undershoot, and non-monotonicity in your DDR interface to improve design quality. Measurements can be validated against JEDEC DDR1/2/3 standard values or custom operating points. The detailed simulations take into account board-level effects, such as lossy transmission lines, reflections, impedance changes, effects of vias, ISI, crosstalk, and timing delays, providing a comprehensive view of your memory interface.

Easy Setup with DDRx Wizard

The HyperLynx DDRx Wizard prompts you with all the key questions necessary to set up simulations, from the simplest DDR designs to the most complicated. Users answer relevant information from a choice of IBIS models for controller and memory devices to drive-strength values for read/write cycles, On-Die-Termination (ODT) settings, and byte-lane / strobe / mask assignment.

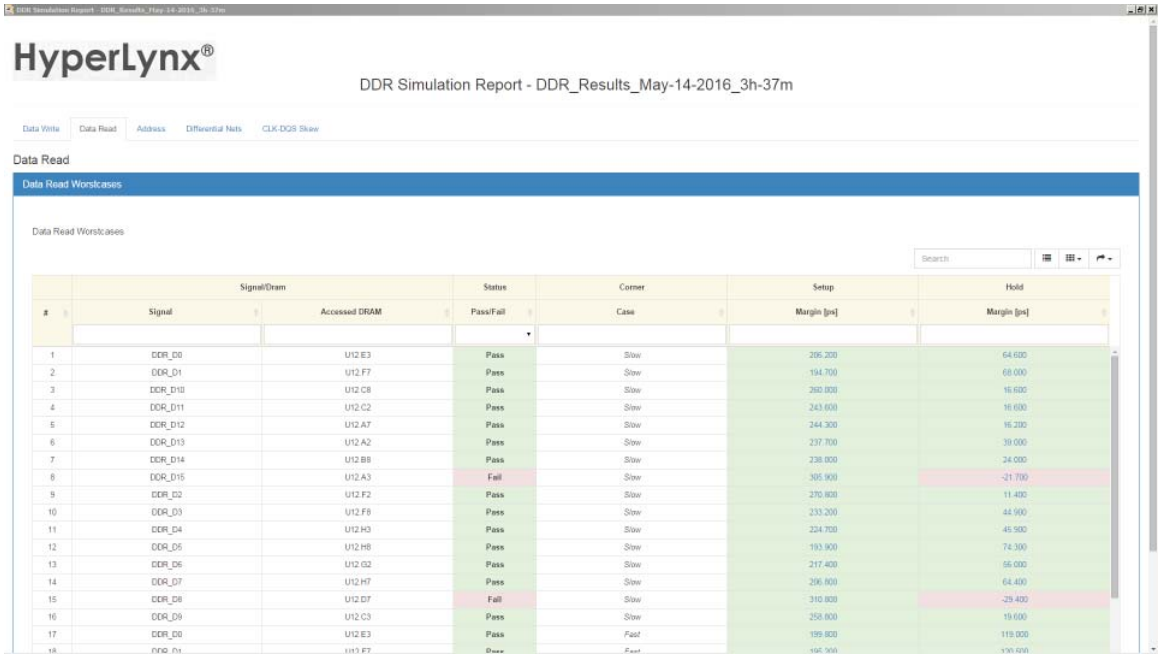
Wizard configurations can be saved and recalled for future use, allowing you and your team to create templates to simulate exactly what you want and to be able to re-use your setups for future designs.



Extensive options in the DDRx Wizard give you flexibility in configuring a DDR simulation.

HTML-based Reports

The DDRx Wizard generates a clean, intuitive report at the end of the simulation process, including pass/fail data, per the information in your wizard-based configuration. Results can be filtered, letting you explore both timing and SI concerns across data read/write cycles, on the address/command bus, or by differential nets. All results in the report are hyperlinked to the relevant simulation data to quickly launch a graphical waveform viewer for the signal(s) in question.



An HTML report makes it easy to intuitively examine results and spot failures. Data can be exported in a variety of formats, according to your needs.

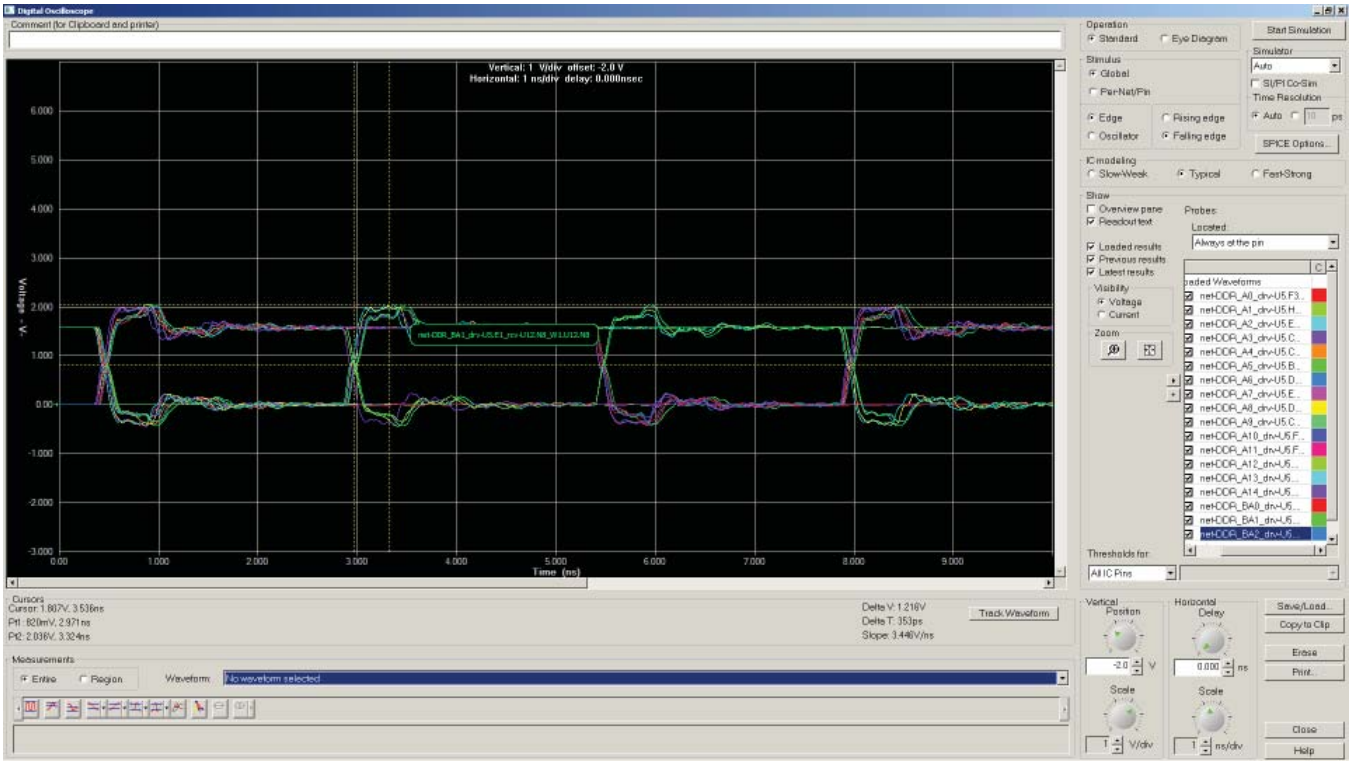
All signals in the simulation results report are hyperlinked and can show a graphical view of the signal.

Detailed, Interactive SI analysis

Batch-mode simulation data created by the DDRx wizard can be saved to disk, so users can examine several nets simultaneously for detailed SI problems offline, using the HyperLynx oscilloscope. Users can interactively place cursors and take notes of overshoot, undershoot or signal timing.

Summary

DDRx bus validation involves the analysis of several timing and voltage measurements. Manual analysis of an entire DDR bus is impractical and error prone. HyperLynx DDRx greatly reduces the setup time required for a successful simulations\ while providing detailed results that can help drive decisions in your design process.



Load any number of signals from batch-mode results into an interactive oscilloscope to take detailed measurements.

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